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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/042,732	04/25/2001	Craig S. Sander	039153-0433 (C167596-CIP)	1672
7590	05/17/2005			EXAMINER NGUYEN, THANH T
				ART UNIT 2813
				PAPER NUMBER

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DATE MAILED: 05/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/042,732	SANDER ET AL.	
	Examiner Thanh T. Nguyen	Art Unit 2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 28 February 2005.

2a) This action is **FINAL**. 2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 19-38 is/are pending in the application.
4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) Claim(s) 19,20 and 25-38 is/are allowed.

6) Claim(s) 21-24 is/are rejected.

7) Claim(s) _____ is/are objected to.

8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) All b) Some * c) None of:
1. Certified copies of the priority documents have been received.
2. Certified copies of the priority documents have been received in Application No. _____.
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) Notice of References Cited (PTO-892)
2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date ____.

4) Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____.
5) Notice of Informal Patent Application (PTO-152)
6) Other: ____.

DETAILED ACTION

Response to Arguments

Applicant's arguments with respect to claims 19-38 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 21-24 are rejected under 35 U.S.C. 102(e) as being anticipated by Tseng (U.S. Patent No. 5,766,998).

Referring to figures 1-8, Tseng teaches an integrated circuit including at least one transistor, the integrated circuit comprising:

A pair of local interconnects (14/16) spaced from each other (see figure 4, col. 4, lines 41-67);

A gate (28) of the transistor disposed in the space between the local interconnects (14/16) and separated from each of the local interconnects by an insulating liner (24), wherein the space

is less than or equal to one minimum lithographic feature (see figure 8, col. 5, lines 14-18, col. 6, lines 22-37).

Regarding to claim 22, the pair of local interconnects (14/16) are spaced form each other by minimum lithographic feature (28, see figure 8).

Regarding to claim 23, the insulating liners (24) are each disposed on an interconnect wall (14/16) adjacent the gate (28) to separate each of the local interconnects (14/16) from the gate (18, see figure 8).

Regarding to claim 24, a source (30) and drain (30) are disposed by at least partially beneath the insulating liners (24, see figure 8).

Claims 21-23 are rejected under 35 U.S.C. 102(e) as being anticipated by Chen et al. (U.S. Patent No. 5,943,564).

Referring to figures 4a-4j, Chen et al. teaches an integrated circuit including at least one transistor, the integrated circuit comprising:

A pair of local interconnects (poly1, 130) spaced from each other (see figure 4 b, col. 3, lines 15-67);

A gate of the transistor (150) disposed in the space between the local interconnects (130) and separated from each of the local interconnects by an insulating liner (142), wherein the space is less than or equal to one minimum lithographic feature (see figures 4b-4h, col. 4, lines 51-67, col. 5, lines 10-32).

Regarding to claim 22, the pair of local interconnects (130) are spaced form each other by minimum lithographic feature (col. 4, lines 51-67, figure 4b).

Regarding to claim 23, the insulating liners (24) are each disposed on an interconnect wall (142) adjacent the gate (150) to separate each of the local interconnects (130) from the gate (see figure 4H).

Allowable Subject Matter

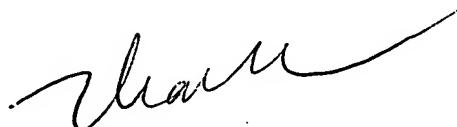
Claims 19-20, 25-38 are allowed over the prior art because none of the prior art alone or in combination teaches a steps of a gate of the transistor disposed in the space between the local interconnects and separated from each of the local interconnects by an insulating liner, wherein the space is less than or equal to the minimum lithographic feature, whereby the width of the transistor is not greater than three of the minimum lithographic features.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh Nguyen whose telephone number is (571) 272-1695, or by Email via address Thanh.Nguyen@uspto.gov. The examiner can normally be reached on Monday-Thursday from 6:00AM to 3:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, can be reached on (571) 272-1702. The fax phone number for this Group is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956 (See **MPEP 203.08**).



Thanh Nguyen
Patent Examiner
Patent Examining Group 2800

TTN